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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,553	09/05/2006	Masatoshi Takahashi	XA-10261	2958

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
KING, DOUGLAS	

ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/521,553	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	DOUGLAS KING	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/12/06, 10/26/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Copy of Machine Translatoin for Japanses 10-198776*.

DETAILED ACTION

Information Disclosure Statement

Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 9/12/06 and 10/26/05. The information disclosed therein was considered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 10, 11, 14, 18, 28 and 29 recite limitations including "through an insulating layer" and the like. It is not understood what is meant by this and appears to be a literal translation of a non-english claim.

Claims 15-16 recite "the first wordline" while parent claim 14 sets forth "the first word lines".

Claims 21 and 22 recite "non-volatile memory holds…information from which stored information is erased." It is not understood what is meant by this limitation.

Claims 19 and 30 recite addition limitations of a channel and control gate and charge storage, etc. while the parent claims set forth similar limitations. It is not understood if these are additional elements or the same elements.

The remaining claims depend from the above and are deficient for at least the same reasons.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1-5, 10, 12-15, 18-23 and 28-31 rejected under 35 U.S.C. 103(a) as being unpatentable over Ishibashi (Japanese Patent Publication 10-198776) in view of Choi (U.S. Patent 5,763,308).

Regarding claims 1, 4, 10, 18, and 28, Ishibashi discloses an IC card being enclosed with a synthetic resin (see Figure 1, 100) comprising: a first non-volatile

memory (see Figure 4, 20) for erasing stored information on a first data length unit; a second non-volatile memory (15) for erasing stored information on a second data length unit; a central processing unit (12); and a terminal for inputting/outputting data from/to an outside (30 or 40), wherein encrypted data (the type or content of the data does not impart structure to a device claim see MPEP section 2114) are input/output from/to the outside, the first non-volatile memory is used for storing an encryption key to be utilized for encrypting the data, the second non-volatile memory is used for storing a program to be processed by the central processing unit (again, the type or content of data is does not structurally distinguish an apparatus claim), each of the first non-volatile memory and the second non-volatile memory has a plurality of non-volatile memory cells (implied by array).

Ishibashi fails to disclose the particular structure of the cells and therefore fails to disclose that each of the non-volatile memory cells has a channel region between a first diffusion layer region and a second diffusion layer region which are formed on the substrate, has an electric charge storage layer on the channel region through a first insulating film, has a first gate terminal on the electric charge storage layer through a second insulating film, and has a second gate terminal through the first gate terminal and a third insulating film on a second channel region which is adjacent to a first channel region provided under the electric charge storage layer,a hot electron generated in the channel region provided under the third insulating film is injected into the electric charge storage layer or an electric charge is extracted from the electric

charge storage layer, thereby carrying out an operation for changing a threshold voltage of the memory cell.

However, Choi discloses such an array wherein each of the non-volatile memory cells has a channel region (see Figure 3, area between 33 and 32 and below 34) between a first diffusion layer region (32 or 33) and a second diffusion layer (other of 32 and 33) region which are formed on the substrate (31), has an electric charge storage layer (34) on the channel region through a first insulating film (see column 3, lines 33+), has a first gate terminal (35) on the electric charge storage layer through a second insulating film, and has a second gate terminal (37) through the first gate terminal and a third insulating film on a second channel region which is adjacent to a first channel region provided under the electric charge storage layer,a hot electron (see claim 1) generated in the channel region provided under the third insulating film is injected into the electric charge storage layer or an electric charge is extracted from the electric charge storage layer, thereby carrying out an operation for changing a threshold voltage of the memory cell (the cells of Choi are capable of being operated in this manner and therefore the limitation is met--see MPEP section 2114).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include memory cells of Choi as the firs and second non-volatile memories of Ishibashi for any of the benefits taught by Choi (see column 5, lines 21+).

Regarding claim 2, Ishibashi as modified above discloses the semiconductor processing device according to claim 1, wherein the first non-volatile memory is further

used for storing information to be utilized for specifying an individual (again, the type of information stored does not impart structure to the claimed device).

Regarding claim 3, Ishibashi as modified above discloses the semiconductor processing device according to claim 2, wherein the first data length is smaller than the second data length(see machine translation of Ishibashi, paragraph 0010).

Regarding claim 5 and 23, Ishibashi as modified above discloses the semiconductor processing device according to claim 4, wherein the central processing unit can give access to the first non-volatile memory and the second non-volatile memory in parallel (the CPU can give access to the first memory while the second memory is still accessible--see Figure 3).

Regarding claim 12, Ishibashi as modified above discloses the IC card according to claim 10 , wherein the central processing unit and the first non-volatile memory are formed on a first semiconductor substrate (see Ishibashi Abstract and Figure 3), the second non-volatile memory is formed on a second semiconductor substrate, and the first non-volatile memory uses a nitride film (see Choi column 3, lines 33+) for a memory cell in order to store data.

Regarding claim 13, Ishibashi as modified above discloses the IC card according to claim 10 or 11, wherein the central processing unit and the first non-volatile memory are formed on a first semiconductor substrate (see Ishibashi Abstract and Figure 3), the second non-volatile memory is formed on a second semiconductor substrate. Ishibashi as modified above fails to disclose that the second non-volatile memory uses a floating gate for a memory cell in order to store data. However,

EEPROM memories employing a floating gate are common and well known in the art and one of ordinary skill would have been aware of the benefits of substituting a floating gate for the nitride layer of Choi.

Regarding claim 14, Ishibashi as modified above discloses the italicised limitations below as outilined in the rejection of claim 10 above: *A semiconductor processing device being capable of inputting/outputting encrypted data to/from an outside comprising:a first non-volatile memory for erasing stored information on a first data length unit;a second non-volatile memory for erasing stored information on a second data length unit; and a central processing unit, wherein each of the first non-volatile memory and the second non-volatile memory has a plurality of memory cells, each of the memory cells has a source region, a drain region and a channel region between the source region and the drain region, has a data storage insulating layer and a first gate on the channel region through an insulating layer, and has a second gate on the data storage insulating layer*, each of the first non-volatile memory and the second non-volatile memory has a plurality of first word lines (see Choi, Figure 5, 1, 2), corresponding memory cells are connected to the first word lines when the stored information is erased from the first non-volatile memory, corresponding memory cells are connected to the first word lines when the stored information is erased from the second non-volatile memory, and the number of the memory cells to be connected to the first word lines in the first non-volatile memory is smaller than that of the memory cells to be connected to the first word lines in the second non-volatile memory (see Ishibashi machine translation, paragraph 0010; second memory is a flash, or block type

erase and first memory is a byte type erase--i.e. second memory has more cells connected for simultaneous ersure).

Regarding claim 15, Ishibashi as modified above discloses the semiconductor processing device according to claim 14, but fails to explicitly disclose that the device further comprising the same number of second word lines as that of the first word lines, the first word line being connected to the second gate of each of the memory cells and the second word line being connected to the first gate of each of the memory cells. However, this just specifies that the array of figure 5 of Choi is a "square" array (i.e. the same number of columns as rows). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the additional rows or columns to create a more dense memory array.

Regarding claims 19, 20, 30 and 31, Inasmuch as the claims are understood, Ishibashi as modified above discloses the semiconductor processing device according to claim 18, wherein the non-volatile memory cell has a source region, a drain region, and a channel region interposed between the source region and the drain region on a semiconductor substrate, a control gate electrode provided through a first insulating film and a memory gate electrode provided through a second insulating film and an electric charge storage insulating film and isolated electrically from the control gate electrode are provided on the channel region(see Choi and rejection of claim 18 above). Ishibashi as modified above is silent on the respective gate breakdown voltage (or, gate insulator breakdown as the gate does not breakdown) and therefore fails to disclose that a gate breakdown voltage of the control gate electrode is lower than that of the memory gate

electrode; and the gate breakdown voltage of the control gate electrode is equal to that of an MOS transistor included in the CPU. However, the gate breakdown voltage is a result effective variable and effects the operational characteristics of the device and it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the respective voltages.

Regarding claims 21 and 22, Ishibashi as modified above discloses the first memory has a shorter data length than the second (see rejections above). The remaining limitations are not understood.

2. Claims 11-13 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishibashi (Japanese Patent Publication 10-198776) in view of Choi (U.S. Patent 5,763,308) as applied to claim 10 above and further in view of Norton (U.S. Patent 6,572,015).

Claims 11 and 29 recite substantially the same limitations as claims 1, 10, 28 rejected above with the addition of an antenna. Ishibasis as modified above fails to disclose an antenna. However, Norton discloses an antenna in conjuction with an IC card for the purpose of wireless communication with an exterior (see Figures 1 and 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the IC card of Ishibashi to include an antenna for wireless communication since such a configuration was known in the art at the time of invention and the modification would yield a predictable result.

Claims 12, 13, 30 and 31 alternatively dependent upon claims 11 and 29 would be rejected in the same manner as those depending from claims 10 and 28 above.

3. Claims 6-9 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishibashi (Japanese Patent Publication 10-198776) in view of Choi (U.S. Patent 5,763,308) as applied to claims 1 and 19 above and further in view of Yamada (Japanese Patent Publication 59-021058).

Regarding claims 6-9 and 24-27, Ishibashi as modified above fails to disclose details of the control portions of the first and second memories and therefore fails to disclose that any portion of the control portion is shared (e.g. sensing amplifiers, voltage generators, and/or decoding circuitry). However, Yamada discloses two memories sharing such circuitry (see Abstract). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to share control circuitry (decoders, voltage generators, and sensing amplifiers) among the first and second memories in order to conserve space.

4. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishibashi (Japanese Patent Publication 10-198776) in view of Choi (U.S. Patent 5,763,308) as applied to claim 14 above and further in view of Lee (U.S. Patent 5,748,538).

Regarding claims 16 and 17, Ishisbashi as modified above discloses the semiconductor processing device according to claim 15, but fails to show the word line

drive circuitry and therefore fails to discloses a switch unit capable of connecting the second gate of a part of the memory cells to be an erasing object of stored information to the first word line when erasing the stored information in the first non-volatile memory. However, switches connection word lines to programming and erasure voltages are well known in the art. Lee shows a word line driver comprising MOS transistors (see Figure 21 for example comprising MOS transistors of both conductivity types).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. DiFillipo (US 2002/0065782); Cocchi (7,43,571); Kocher (6,289,455) and Ledford (US 2002/0174382) disclose various embodiments of IC cards with memory chips.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DOUGLAS KING whose telephone number is (571)272-2311. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Douglas King/
Examiner, Art Unit 2824

/VanThu Nguyen/
Primary Examiner, Art Unit 2824